RESPONSE

Claims 1-4, 7-15, and 19-26 are currently pending in the Application. In the Office Action, the Examiner notes that all previous grounds of rejection with respect to the currently pending claims have been withdrawn. Claims 20-26 are allowed.

Claims 1, 3, 4, 7, 8, 10-14 and 19 stand rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 5,963,745 to Collins et al ("Collins"). Furthermore, claims 2, 9 and 15 stand objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims.

Applicants hereby amend claims 1, 2 and 14 without any intention of disclaiming any equivalents thereof. Support for the amendments to claims 1, 2 and 14 may be found in the specification as described below.

Upon entry of this paper, claims 1-4, 7-15 and 19-26 will be pending in this application. Reconsideration is respectfully requested.

Rejections Under 35 U.S.C. §102

Claims 1,3,4,7,8,10-14 and 19 stand rejected under 35 U.S.C. §102(b) as being anticipated by US Patent No. 5,967,745 to Collins.

Collins

Generally, Collins teaches a parallel array processing system which "forms a basis for the systems described which are capable of massively parallel processing of complex scientific and business applications"(Col 2, lines 56-59). The parallel array processing architecture disclosed in Collins executes single or multiple instruction streams on multiple data streams in each processing element simultaneously. According to Collins, the parallel array processing system can "function in either SIMD or MIMD mode, in dual SIMD/MODE, with asynchronous processing, and with SIMIMD functionality" (Col 12, lines 20-24).

SIMD is a processor array architecture wherein "all processors in the array are commanded from a Single Instruction stream to execute Multiple Data streams located one per processing element" (emphasis added) (Col 7 lines 52-55). MIMD refers "to a processor array architecture wherein each processor in the array has its own instruction stream, thus Multiple Instruction stream, to execute Multiple Data streams located one per processing element" (emphasis added) (Col 5 lines 61-64). Finally, "SIMIMD is a processor architecture wherein all processors in the array are commanded from a Single Instruction stream, to execute Multiple Data streams located one per processing element. Within this construct, data dependent operations within each picket that mimic instruction execution are controlled by the SIMD instruction stream."(emphasis added) (Col 8, lines 7-13).

Thus the stress in Collins is on "multiple data streams" and multiple data streams are a significant part of the invention. This is because, as stated above, Collins describes a system for the massively parallel processing of complex scientific and business applications and as such each processor has its own data set to work on.

Identical Data Streams Distinction

An initial basis for distinction between the claimed invention and Collins lies in the fact that the claims, as amended, refer to multiple data processing elements which each execute substantially identical instruction streams on identical data streams at the same time.

Specifically, amended independent claim 1 recites, in part:

> "a plurality of data processing elements executing substantially identical instruction streams on identical data streams substantially simultaneously;"

Similarly, independent claim 14, as amended recites, in part:

> "generating, by a plurality of data processing elements, identical transactions on identical data streams, each transaction having an I/O node address;"

Thus both claims recite executing substantially identical instruction streams or transactions on identical data streams substantially simultaneously. This is significant because Applicants' invention relates to fault tolerant computing in which each processor operates on exactly the same data with the same instruction set. In this way, results can be compared and errors detected.

As indicated in the instant specification: "the I/O subsystem 26 continues to forward input data streams sent by the peripheral devices to the CPU boards 22 and 22'."(Paragraph 54)

and

> "The present invention relates to apparatus and methods for fault-tolerant computing using an asynchronous switching fabric architecture that increases the aggregate data rate between system components, maximizing overall I/O throughput by handling multiple I/O streams simultaneously. One embodiment of the invention comprises a plurality of redundant data processing elements where each of the redundant data processing elements is executing substantially identical instructions substantially simultaneously.".(Paragraph 7)

In contrast, Collins does not teach redundant data processing elements executing instructions on identical data streams in this manner. The end goal of Collins is to have a system that is capable of faster and more efficient super-computing by dividing the input data across many processors in order to solve complex problems. As Collins states:

> "In the never ending quest for faster computers, engineers are linking hundreds, arid [sic] even thousands of low cost microprocessors together in parallel to create super supercomputers that divide in order to conquer complex problems that stump today's machines. Such machines are called massively parallel. We have created a new way to create massively parallel systems. The many improvements which we have made should be considered against the background of many works of others." (Col 8, lines 48-57).

Thus, unlike the present invention, the Collins invention seeks to have multiple processors operate on different data streams to achieve parallel processing while the present invention seeks to have multiple processors operate on the same data stream to achieve reliability.

The Applicants submit that the prior art of record neither teaches nor suggests a system in which a plurality of data processing elements execute substantially identical instruction streams on identical data streams substantially simultaneously, and which has an I/O node in communication with at least one of the plurality of data processing elements and a switching fabric communicating transactions asynchronously between at least one of the plurality of data processing elements and the I/O node.

Conclusion

Applicants submit therefore that claims 1 and 14 are allowable as amended. Applicants also submit that claims 3, 4, 7, 8, 10-13 and 19 are allowable at least for the reason that they depend on allowable base claims.

Claims 2, 9 and 15 stand objected to but would be allowable if amended to incorporate the language of their base claim and all intervening claims. Applicants herein amend claim 2 to incorporate the language of its base claim, claim 1, and is therefore allowable as amended. Applicants submit that claims 9 and 15 are allowable as depending from now allowable base claims 1 and 14.

Applicants submit that all claims are now in condition for allowance and request early favorable action by the Examiner.

If, in the Examiner's opinion, a telephonic interview would expedite the favorable prosecution of the present application, the undersigned attorney would welcome the opportunity to discuss any outstanding issues, and to work with the Examiner toward placing the application in condition for allowance.

Respectfully submitted,

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